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Honeywell

Military & Space Products

32K x 8 ROM—SOI

HX6656

FEATURES

RADIATION

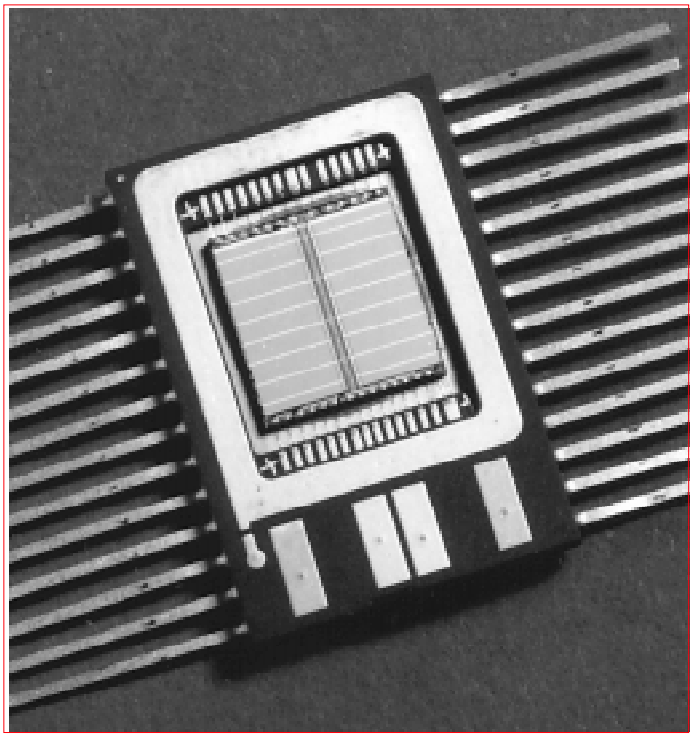
- Fabricated with RICMOS™ IV Silicon on Insulator (SOI) 0.75 µm Process (L_{eff} = 0.6 µm)
- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad(Si)/s
- Dose Rate Survivability through $1x10^{11}$ rad(Si)/s
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- SEU Immune
- Latchup Free

OTHER

- Read Cycle Times
  ≤ 17 ns (Typical)
  ≤ 25 ns (-55 to 125°C)
- Typical Operating Power <15 mW/MHz
- Asynchronous Operation
- CMOS or TTL Compatible I/O
- Single 5 V ± 10% Power Supply
- Packaging Options
  - 28-Lead Flat Pack (0.500 in. x 0.720 in.)
  - 28-Lead DIP, MIL-STD-1835, CDIP2-T28
  - 36-Lead Flat Pack (0.630 in. x 0.650 in.)

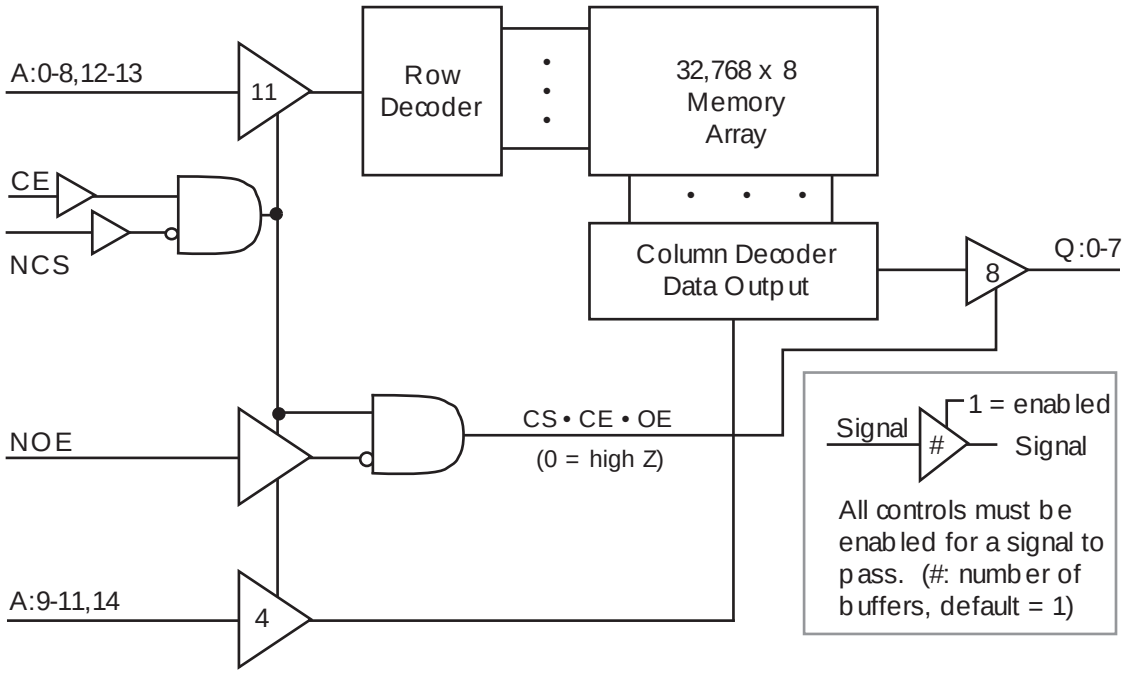
GENERAL DESCRIPTION

The 32K x 8 Radiation Hardened ROM is a high performance 32,768 word x 8-bit read only memory with industry-standard functionality. It is fabricated with Honeywell's radiation hardened technology, and is designed for use in systems operating in radiation environments. The ROM operates over the full military temperature range and requires only a single 5 V ± 10% power supply. The ROM is available with either TTL or CMOS compatible I/O. Power consumption is typically less than 15 mW/MHz in operation, and less than 5 mW when de-selected. The ROM operation is fully asynchronous, with an associated typical access time of 14 ns.



Honeywell's enhanced SOI RICMOS™ IV (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The RICMOS™ IV process is a 5-volt, SIMOX CMOS technology with a 150 Å gate oxide and a minimum drawn feature size of 0.75 µm (0.6 µm effective gate length—L_{eff}). Additional features include tungsten via plugs, Honeywell's proprietary SHARP planarization process, and a lightly doped drain (LDD) structure for improved short channel reliability.

FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-14 Address input pins which select a particular eight-bit word within the memory array.

Q: 0-7 Data Output Pins.

NCS Negative chip select, when at a low level allows normal read operation. When at a high level NCS forces the ROM to a precharge condition, holds the data output drivers in a high impedance state and disables all input buffers except CE. If this signal is not used it must be connected to VSS.

NOE Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS and CE. If this signal is not used it must be connected to VSS.

CE* Chip enable, when at a high level allows normal operation. When at a low level CE forces the ROM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except the NCS input buffer. If this signal is not used it must be connected to VDD.

TRUTH TABLE

NCS	CE*	NOE	MODE	Q
L	H	L	Read	Data Out
H	X	XX	Deselected	High Z
X	L	XX	Disabled	High Z

*Not Available in 28-lead DIP or 28-Lead Flat Pack

Notes:
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X, CE=X

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The ROM will meet all stated functional and electrical specifications over the entire operating temperature range after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and ROM product using 10 keV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 keV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The ROM is capable of reading and retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤1 µs duration up to $1x10^9$ rad(Si)/s, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation (timing degradation during transient pulse radiation is ≤10%), it is suggested that stiffening capacitance be placed on or near the package VDD and VSS, with a maximum inductance between the package (chip) and stiffening capacitance of 0.7 nH per part. If there are no operate-through requirements, typical circuit board mounted de-coupling capacitors are recommended.

The ROM will meet any functional or electrical specification after exposure to a radiation pulse of ≤50 ns duration up to $1x10^{11}$ rad(Si)/s, when applied under recommended operating conditions.

Neutron Radiation

The ROM will meet any functional or timing specification after a total neutron fluence of up to $1x10^{14}$ cm^{-2} applied under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Single Event Phenomena

All storage elements within the ROM are immune to single event upsets. No access time or other performance degradation will occur for LET 190 MeV/cm/mg^2.

Latchup

The ROM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

RADIATION HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	≥$1x10^6$	rad(SiO_2)	T_A=25°C
Transient Dose Rate Upset (3)	≥$1x10^9$	rad(Si)/s	Pulse width ≤1 µs
Transient Dose Rate Survivability (3)	≥$1x10^{11}$	rad(Si)/s	Pulse width ≤50 ns, X-ray, VDD=6.0 V, T_A=25°C
Neutron Fluence	≥$1x10^{14}$	N/cm^2	1 MeV equivalent energy, Unbiased, T_A=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to 125°C.
(3) Not guaranteed with 28–Lead DIP.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating		Units
			Min	Max	
VDD	Positive Supply Voltage (2)		-0.5	7.0	V
VPIN	Voltage on Any Pin (2)		-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)		-65	150	°C
TSOLDER	Soldering Temperature • Time			270•5	°C•s
PD	Total Package Power Dissipation (3)			2.5	W
IOUT	DC or Average Output Current			25	mA
VPROT	ESD Input Protection Voltage (4)		2000		V
ΘJC	Thermal Resistance (Jct-to-Case)	28 FP/36 FP		2	°C/W
		28 DIP		10	
TJ	Junction Temperature			175	°C

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) ROM power dissipation (IDDSB + IDDOP) plus ROM output driver power dissipation due to external loading must not exceed this specification.
(4) Class 2 electrostatic discharge (ESD) input protection. Tested per MIL-STD-883, Method 3015 by DESC certified lab.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

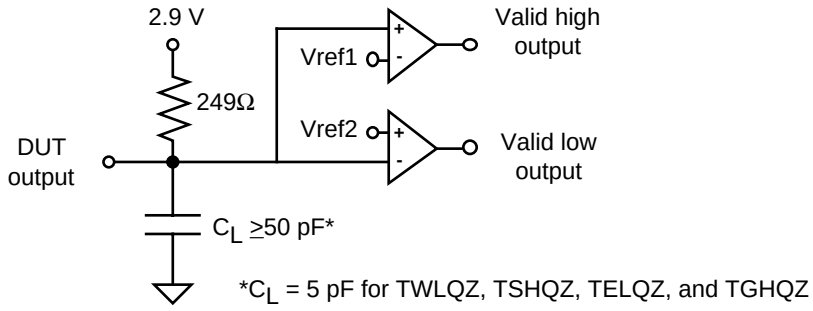
Symbol	Parameter	Typical (1)	Worst Case		Units	Test Conditions
			Min	Max		
CI	Input Capacitance			7	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance			9	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions
IDDSB1	Static Supply Current			1.5	mA	VIH=VDD IO=0 VIL=VSS Inputs Stable
IDDSBMF	Standby Supply Current - Deselected			1.5	mA	NCS=VDD, IO=0, f=40 MHz
IDDOPR	Dynamic Supply Current, Selected			4.0	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS
II	Input Leakage Current		-1	+1	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current		-1	+1	µA	VSS≤VIO≤VDD Output=high Z
VIL	Low-Level Input Voltage CMOS TTL			0.3xV_{DD} 0.8	V V	 VDD = 4.5V
VIH	High-Level Input Voltage CMOS TTL		0.7xV_{DD} 2.2		V V	 VDD = 5.5V
VOL	Low-Level Output Voltage			0.4 0.05	V V	VDD = 4.5V, IOL = 10 mA VDD = 4.5V, IOL = 200 µA
VOH	High-Level Output Voltage		4.2 V_{DD}-0.05		V V	VDD = 4.5V, IOH = -5 mA VDD = 4.5V, IOH = -200 µA

(1) Typical operating conditions: VDD= 5.0 V,TA=25°C, pre-radiation.
(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55°C to +125°C, post total dose at 25°C.
(3) All inputs switching. DC average current.

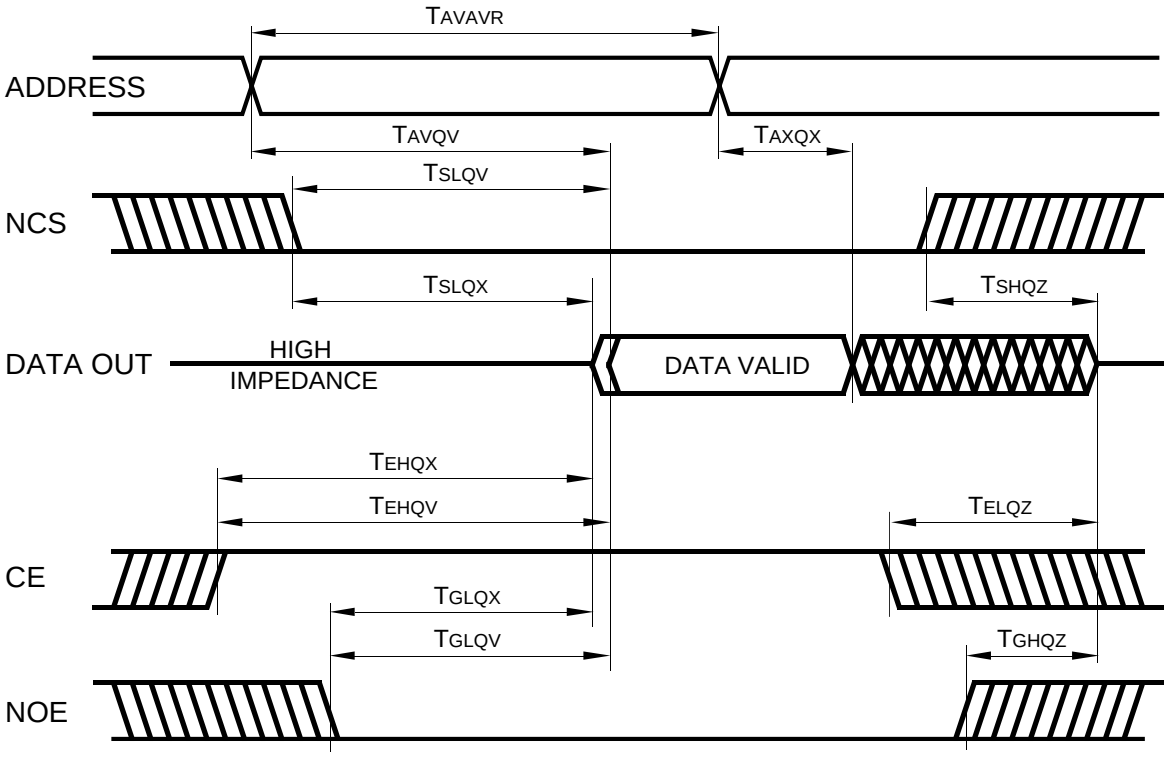


Tester Equivalent Load Circuit

READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Worst Case (3) -55 to 125°C Max	Units
TAVAVR	Address Read Cycle Time		25		ns
TAVQV	Address Access Time			25	ns
TAXQX	Address Change to Output Invalid Time		3		ns
TSLQV	Chip Select Access Time			25	ns
TSLQX	Chip Select Output Enable Time		5		ns
TSHQZ	Chip Select Output Disable Time			10	ns
TEHQV	Chip Enable Access Time (4)			25	ns
TEHQX	Chip Enable Output Enable Time (4)		5		ns
TELQZ	Chip Enable Output Disable Time (4)			10	ns
TGLQV	Output Enable Access Time			9	ns
TGLQX	Output Enable Output Enable Time		0		ns
TGHQZ	Output Enable Output Disable Time			9	ns

(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading $C_L \geq 50$ pF, or equivalent capacitive output loading C_L=5 pF for TSHQZ, TELQZ TGHQZ. For C_L >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55°C to +125°C, post total dose at 25°C.
(4) Chip Enable (CE) pin not available on 28-lead FP or DIP.



DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

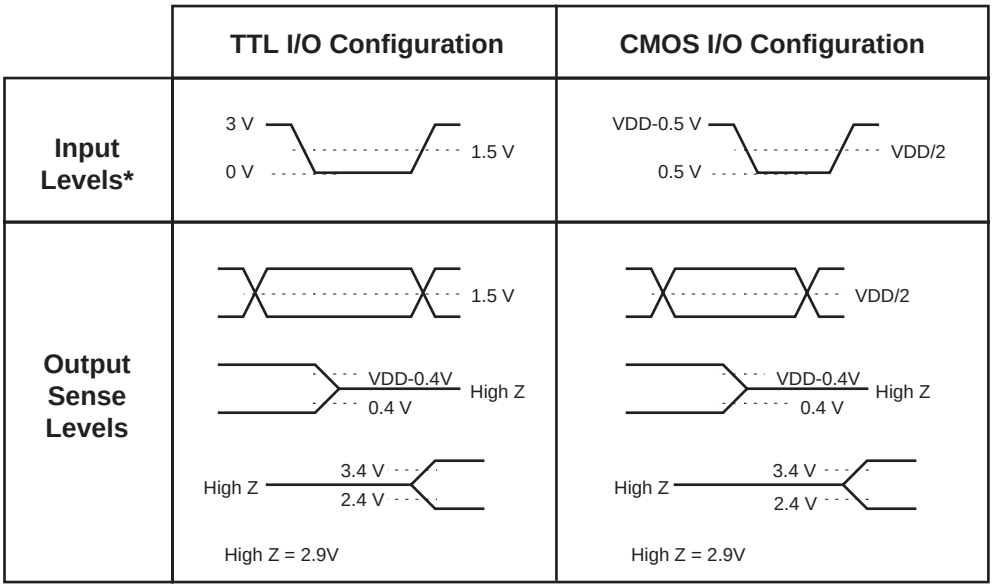
The ROM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with CE held continuously high, and toggling the addresses.

For an address activated read cycle, NCS and CE must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the ROM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses and CE must be valid prior to or coincident with the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS, however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.

TESTER AC TIMING CHARACTERISTICS



* Input rise and fall times <1 ns/V

QUALITY AND RADIATION HARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete “Total Quality Assurance System,” a computer data base process performance tracking system, and a radiation-hardness assurance strategy.

The radiation hardness assurance strategy starts with a technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by irradiating test structures as well as product die, and then monitoring key parameters which are sensitive to ionizing radiation. Conventional MIL-STD-883C TM 5005 Group E testing, which includes total dose exposure with Cobalt 60, may also be performed as required. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

SCREENING LEVELS

Honeywell offers several levels of device screening to meet your system needs. “Engineering Devices” are available with limited performance and screening for breadboarding and/or evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883. As a QML supplier, Honeywell also offers QML Class Q and V devices per MIL-PRF-38535 and are available per the applicable Standard Military Drawing (SMD). QML devices offer ease of procurement by eliminating the need to create detailed specifications and offer benefits of improved quality and cost savings through standardization.

RELIABILITY

Honeywell understands the stringent reliability requirements for space and defense systems and has extensive experience in reliability testing on programs of this nature. This experience is derived from comprehensive testing of VLSI processes. Reliability attributes of the RICMOS™ process were characterized by testing specially designed irradiated and non-irradiated test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure more reliable products.

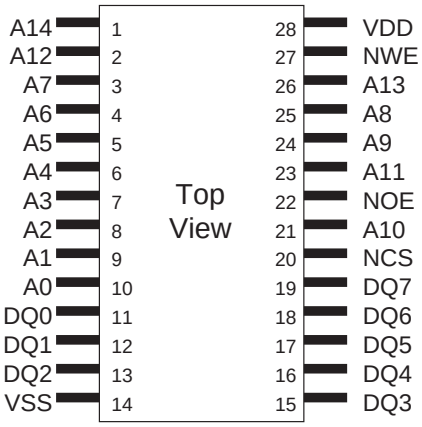
In addition, the reliability of the RICMOS™ process and product in a military environment was monitored by testing irradiated and non-irradiated circuits in accelerated dynamic life test conditions. Packages are qualified for product use after undergoing Groups B & D testing as outlined in MIL-STD-883, TM 5005, Class S. The product is qualified by following a screening and testing flow to meet the customer’s requirements. Quality conformance testing is performed as an option on all production lots to ensure the ongoing reliability of the product.

PACKAGING

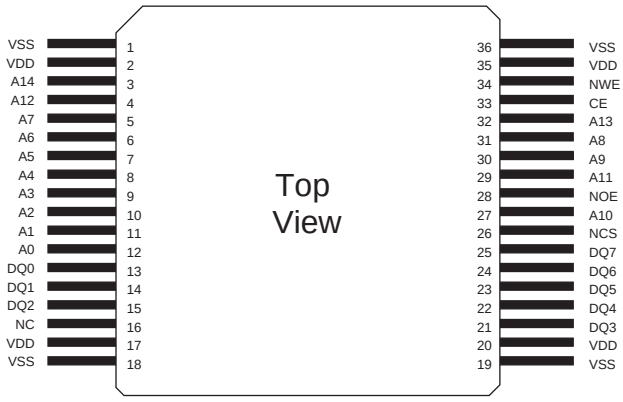
The 32K x 8 ROM is offered in a custom 36-lead flat pack (FP), 28-Lead FP, or standard 28-lead DIP. Each package is constructed of multilayer ceramic (Al_2O_3) and features internal power and ground planes. The 36-lead FP also features a non-conductive ceramic tie bar on the lead frame. The tie bar allows electrical testing of the device, while preserving the lead integrity during shipping and handling, up to the point of lead forming and insertion.

Ceramic chip capacitors can be mounted to the package to maximize supply noise decoupling and increase board packing density. These capacitors attach directly to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package. All NC (no connect) pins should be connected to VSS to prevent charge build up in the radiation environment.

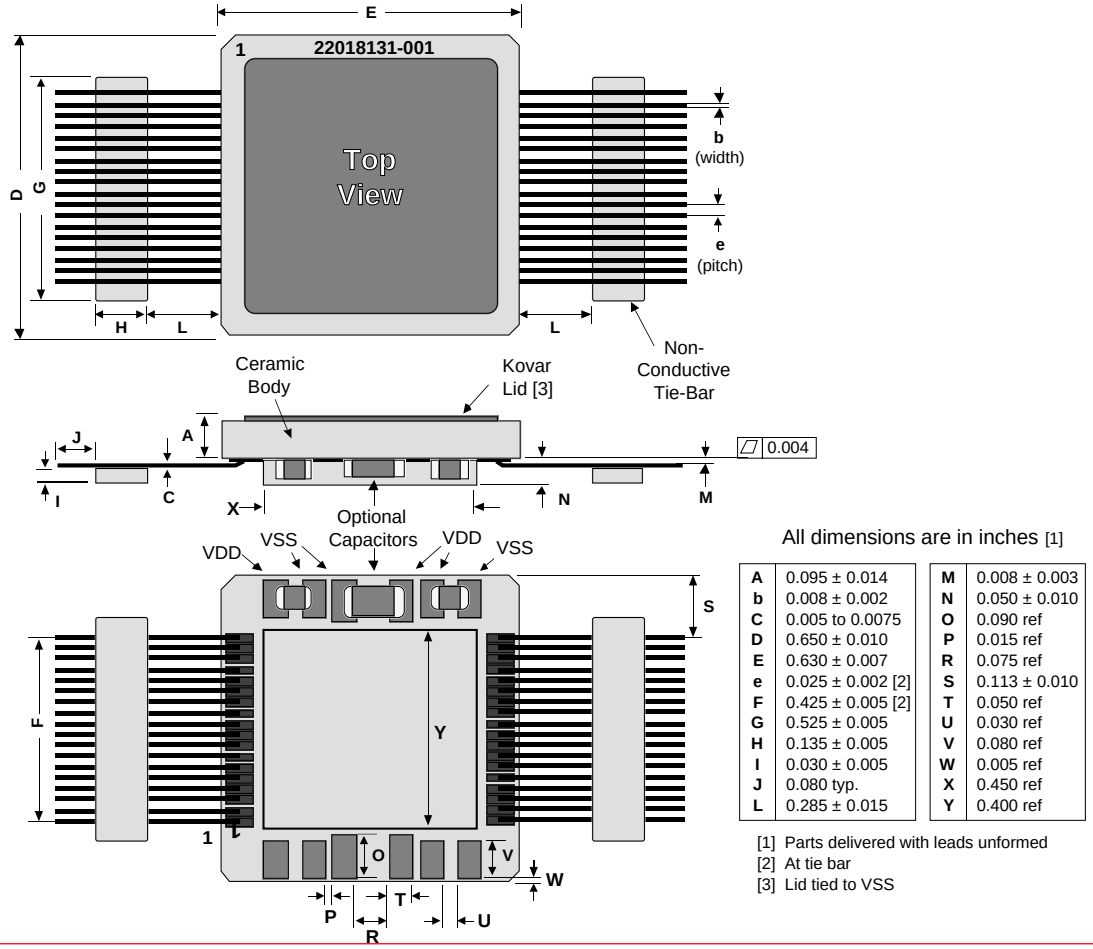
28-LEAD FP PINOUT



36-LEAD FP PINOUT



36-LEAD FLAT PACK

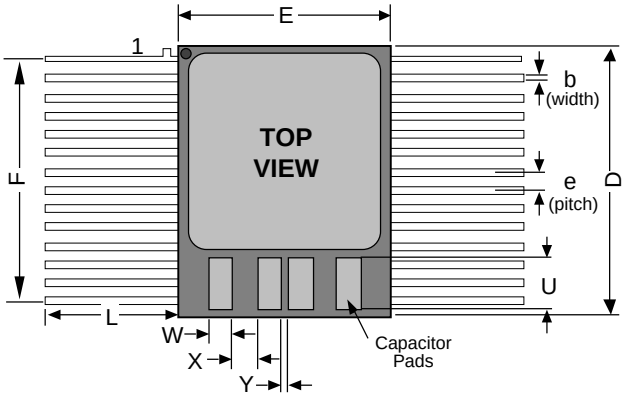


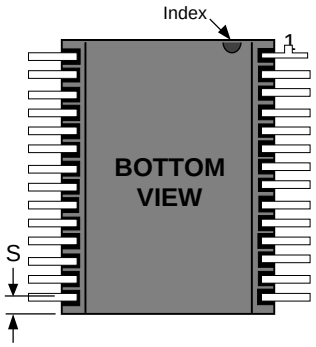
All dimensions are in inches [1]

A	0.095 ± 0.014	**M**	0.008 ± 0.003
b	0.008 ± 0.002	**N**	0.050 ± 0.010
C	0.005 to 0.0075	**O**	0.090 ref
D	0.650 ± 0.010	**P**	0.015 ref
E	0.630 ± 0.007	**R**	0.075 ref
e	0.025 ± 0.002 [2]	**S**	0.113 ± 0.010
F	0.425 ± 0.005 [2]	**T**	0.050 ref
G	0.525 ± 0.005	**U**	0.030 ref
H	0.135 ± 0.005	**V**	0.080 ref
I	0.030 ± 0.005	**W**	0.005 ref
J	0.080 typ.	**X**	0.450 ref
L	0.285 ± 0.015	**Y**	0.400 ref

[1] Parts delivered with leads unformed
[2] At tie bar
[3] Lid tied to VSS

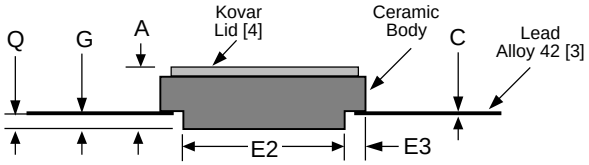
28-LEAD FLAT PACK (22017842-001)





All dimensions in inches

A	0.105 ± 0.015
b	0.017 ± 0.002
C	0.003 to 0.006
D	0.720 ± 0.008
e	0.050 ± 0.005 [1]
E	0.500 ± 0.007
E2	0.380 ± 0.008
E3	0.060 ref
F	0.650 ± 0.005 [2]
G	0.035 ± 0.004
L	0.295 min [3]
Q	0.026 to 0.045
S	0.045 ± 0.010
U	0.130 ref
W	0.050 ref
X	0.075 ref
Y	0.010 ref

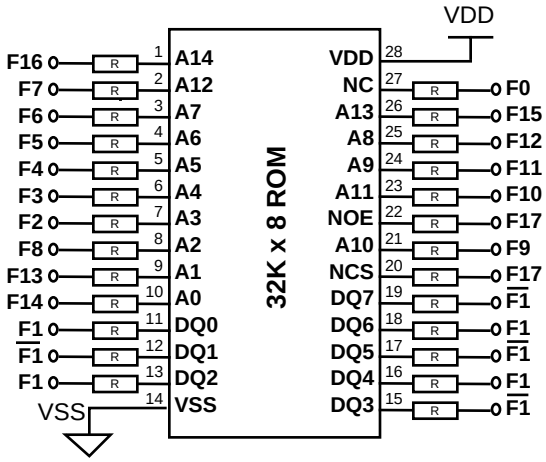


[1] BSC – Basic lead spacing between centers
[2] Where lead is brazed to package
[3] Parts delivered with leads unformed
[4] Lid connected to VSS

28-LEAD DIP (22017785-001)

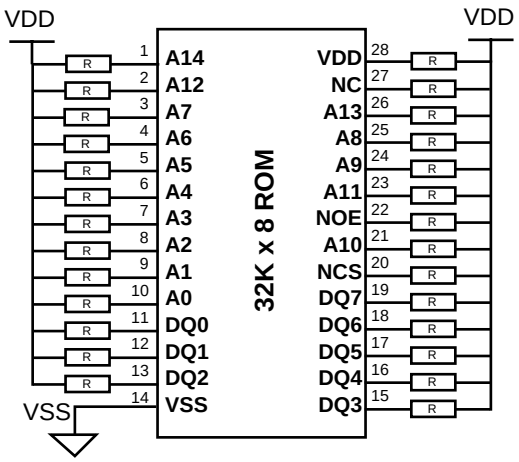
For 28-Lead DIP description, see MIL-STD-1835, Type CDIP2-T28, Config. C, Dimensions D-10

DYNAMIC BURN-IN DIAGRAM*



VDD = 6.5V, R ≤ 10 KΩ, VIH = VDD, VIL = VSS
Ambient Temperature ≥ 125 °C, F0 ≥ 100 KHz Sq Wave
Frequency of F1 = F0/2, F2 = F0/4, F3 = F0/8, etc.

STATIC BURN-IN DIAGRAM*



VDD = 5.5V, R ≤ 10 KΩ
Ambient Temperature ≥ 125 °C

*36-lead Flat Pack burn-in diagrams have similar connections and are available on request.

ROM CODE

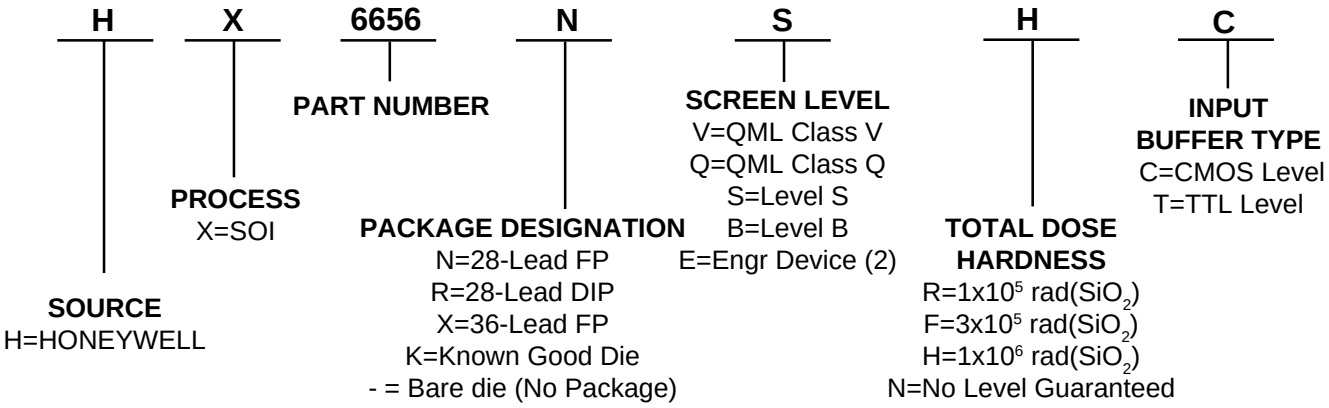
The ROM code can be provided to Honeywell via FTP, E-Mail or a variety of magnetic storage media, including 3.5 inch floppy disc, 4m digital tape and others.

The ROM Code data file should contain the following format:

<address> [/] <data> [;] [Comment]
Where items enclosed in '[‘and’]' are optional.
The address and data must be hex numbers in the form, MSB...LSB. The "/" and the ";" are optional and any characters after the "#" are comments. For example the following input file, all of the lines are valid:

000 d4
001 / 32
002 1d
003 / 72;
4/5e; # all of these lines are in valid format

ORDERING INFORMATION (1)



(1) Orders may be faxed to 612-954-2051. Please contact our Customer Logistics Department at 612-954-2888 for further information.
(2) Engineering Device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, no radiation guaranteed.
Contact Factory with other needs.

To learn more about Honeywell Solid State Electronics Center, visit our web site at http://www.ssec.honeywell.com

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